

# Design and Simulation of Novel Single-Input Sampling Instance Control Circuit

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## Abstract

This paper proposes a novel single-input sampling instance control circuit used in primary-side controller of Switch Mode Power Supplies (SMPS) without optical-coupler and secondary feedback control circuit. The novel control circuit is based on the idea determining the sampling instance of current switching cycle by the duration of the voltage pulse at the auxiliary winding during the previous switching cycle. So the sampling instance is always kept constant, as long as the duration of the voltage pulse is not changed. The control deviations resulting from changeful parameters can be reduced. Thus, high controlling accuracy can be achieved. According to the design, the width of the sampling signal is adjustable, which enlarges the range of application. Besides, the characteristic of single-input makes the obtaining of input signal easy.

## Keyword

fly-back ; Switch Mode Power Supply; auxiliary winding; sampling instance

## 1. Introduction

With the advantages of high efficiency, smaller size and lighter weight [1], switch mode power supplies (SMPS) have been widely used in electronic appliances, computers, etc. For safety reasons and low cost, primary-side controlled SMPS without optical-coupler and secondary feedback control circuit usually derives feedback from an auxiliary winding [2]. As the only control unit of such SMPS, primary-side controller is vital to the whole power supply system. Thus, its design is challenging and complicated. The primary-side controller related by this paper operates in Discontinuous Conduction Mode (DCM). It adjusts the output to the load by changing the switching frequency

realized by controlling the dead-time [3]. Each period the controlled variable is sampled and hold before the dead-time coming. The sampling instance is of great significance for the performance of the controller. So it is important to control the sampling instance accurately.

This paper firstly introduces the principle of primary-side controlled SMPS without the optical-coupler and secondary feedback control circuit and brings forward why such a controller needs a sampling instance control circuit. Next it enumerates the prior methods and points out the shortages of the prior design. Then it proposes a novel single-input control circuit and describes the detailed operation of the control circuit. Finally the characteristics of the novel control circuit are presented.

## 2. Principle of primary-side controlled SMPS

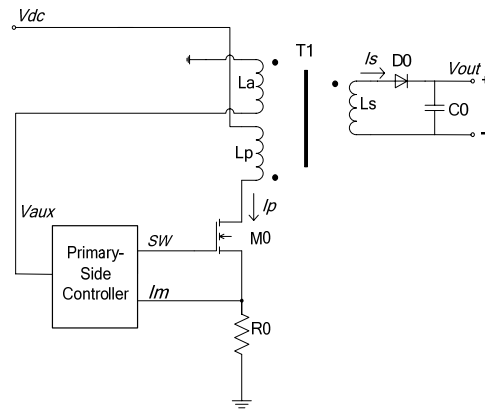


Figure 1. Typical circuit of primary-side controlled SMPS

Figure 1 illustrates a typical circuit of primary-side controlled SMPS which comprises a primary-side controller, a primary switch and a transformer with an

auxiliary winding. The controlled variable is transferred by the auxiliary winding from the secondary to the primary side. When the primary switch is opened, a voltage pulse is induced within the auxiliary winding. Since the value of the voltage pulse is correlated with the output voltage, as the output voltage in the secondary side varies due to the variation of the load, a proportional variation will be induced in the auxiliary winding as well [4]. It is concluded that the voltage pulse at the auxiliary winding contains the information of output voltage and the load. So it can be taken into account of controlling the output power. If the current through the secondary winding reaches zero during OFF time, the supply is said to operate in Discontinuous Conduction Mode (DCM). The voltage pulse is only present before the current in the secondary winding decreases to zero. But it is needed to control the duration of the current staying at a null level and determine when the primary switch is closed again [5]. So a sample and hold circuit is designed to hold the voltage level for the phase of current flow and pause. Due to the decreasing of the current through the secondary winding, the sampling instance should be relative constant to the duration of the voltage pulse. Thereby an accurate sampling instance control circuit is necessary.

### 3. Description of prior methods

In prior primary-side controlled SMPS design [6], a method is implied that each period the sampling signal is generated after a fixed interval with respect to the opening of the switch. The disadvantage of this method is that the form of the voltage pulse at the auxiliary winding is greatly influenced by different operation parameters such as input voltages, output load, and disturbances. So the sampling instance is of great significance for the performance of primary controller. Obviously a fixed value for the sampling instance limits the application range for such a switch mode power supply unit strongly.

Another prior primary-side controlled SMPS design [7] proposes a new method to define the sampling instance that determining the sampling instance of the current switching cycle based on the duration of the voltage pulse at the auxiliary winding during the previous switching cycle. This method is extraordinary practicable because a new idea is issued that controlling the next state with the current state instead of the original state. Thereby, the controlling is instant. The controlled variable is corrected every period. Therefore high controlling accuracy can be achieved.

Based on the second method, the paper proposes a novel single-input sampling instance control circuit. It just needs one input signal generated by a comparator which detects both the beginning and end of the voltage pulse at the auxiliary winding. And, withal, the width of the sampling signal is adjustable by altering the value of the internal capacitor.

### 4. Novel single-input sampling instance control circuit arrangement

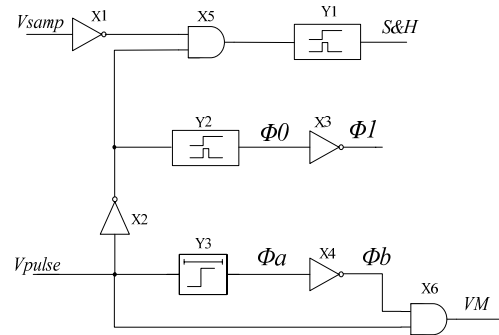


Figure 2a. The digital controller of the control circuit

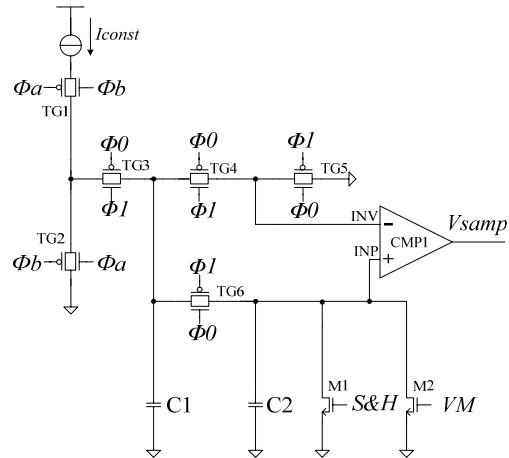
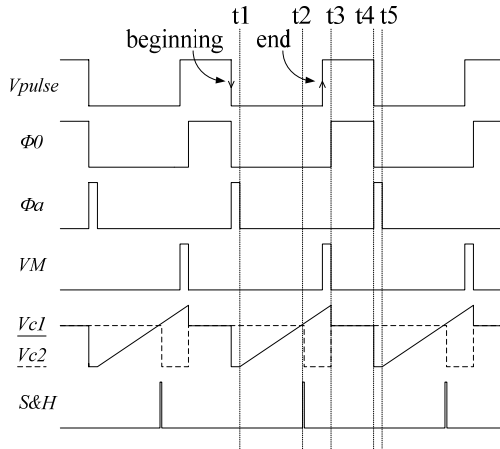


Figure 2b. The switch network of the control circuit

The novel single-input sampling instance control circuit is formed by a digital controller (figure 2a) and a switch network (figure 2b). The signals in two figures named the same stand for the same signals.  $V_{pulse}$  is the only input signal which is converted from the voltage pulse at the auxiliary winding, whose falling edge represents the beginning of the voltage pulse and rising edge represents the end of the voltage pulse. The signal  $S\&H$  is the final output, which determines the sampling instance. In figure 2a, Y1 and Y2 are rising edge pulse generators defined

that it will generate a positive pulse whose width is determined by internal capacitor when a rising edge comes, Y3 is a rising edge delay unit defined that the output signal delays a short time which is determined by internal capacitor at the rising edge of a voltage pulse but is synchronous at the falling edge. Figure 2b is formed by a comparator CMP1, transmit-gates TG1 to TG6, switches M1 and M2 and capacitors C1 and C2. The signal  $\Phi a$  and  $\Phi 0$  is inverse to the signal  $\Phi b$  and  $\Phi 1$  respectively. That means when TG1 is opened, TG2 is closed and when TG3 and TG4 are opened, TG5 and TG6 are closed. The opposite is alike.

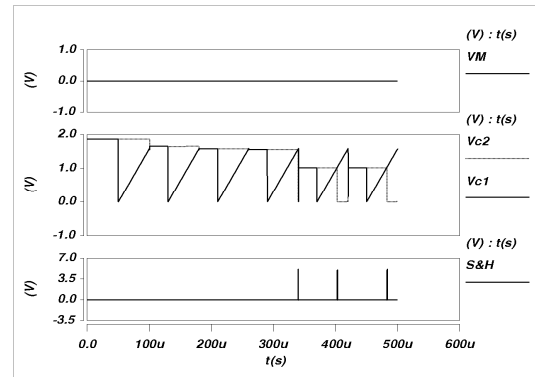


**Figure 3.** The main waveforms of the control circuit

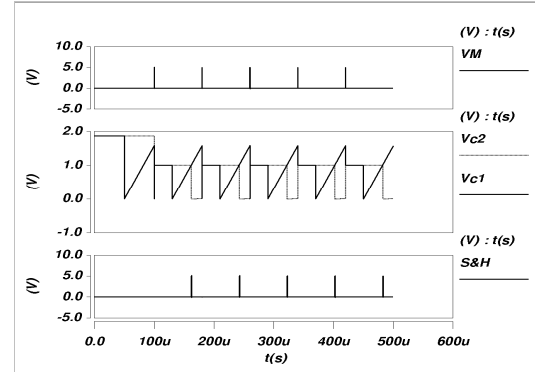
Figure 3 is the main waveforms of the control circuit. At the moment t1, TG1, TG3 and TG4 are closed. The capacitor C1 is connected with the constant current source  $I_{const}$  and is charged subsequently. The voltage at capacitor C1 is compared with the one at capacitor C2 by means of the comparator CMP1. When the voltage at capacitor C1 reaches the value of the voltage at capacitor C2 at the moment t2, the comparator CMP1 outputs a rising edge signal  $V_{samp}$ , in response to which the rising edge pulse generator unit Y1 outputs a short positive pulse **S&H**. Simultaneously, the capacitor C2 is short circuited and discharged via the switch M1. The capacitor C1 is further charged by means of the constant current source  $I_{const}$  until the moment t3. At this moment, TG1, TG5 and TG6 are closed. The charging of capacitor C1 is brought to an end and the two capacitors C1 and C2 are connected in parallel. The charge at capacitor C1 is shared by capacitor C2 [8]. The voltage  $V_{c2}$  after sharing is equal to  $V_{c1} \times C1 / (C1 + C2)$ . If we choose the capacity values in a way that  $C1 = K \times C2$ , the final result is  $V_{c2} = V_{c1} \times K / (K + 1)$ .

At the moment t4, TG2, TG3 and TG4 are closed. The two capacitors are separated and capacitor C1 is

connected to the ground and discharged. With the coming of the moment t5 the next switching cycle starts. Noticed that the pulse of signal  $\Phi a$  is quite short (for convenience of explaining it is figured in an exaggerated way). Thus, the moment t1 and t5 approximately represents the beginning of two switching cycles separately. According to the design it is obvious that the sampling instance lies on when the voltage at capacitor C1 is charged to the voltage  $V_{c2}$  stored in the last switching cycle.



**Figure 4a.** The simulation results without the switch M2 controlled by signal **VM**



**Figure 4b.** The simulation results with the switch M2 controlled by signal **VM**

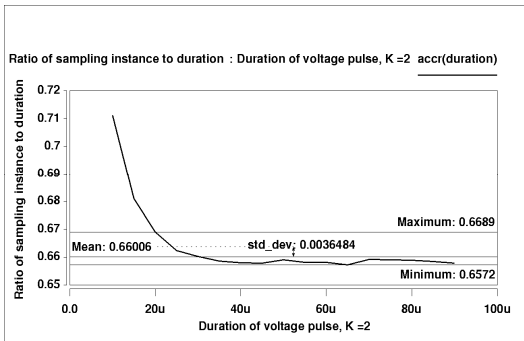
Hereto, the arrangement of the control circuit seems finished. There is another problem: it is not assured that the capacitor C2 has been discharged before capacitors C1 and C2 sharing their charge if the sampling signal **S&H** does not come, for example, at the startup of the circuit. The status continues until the first sampling signal coming and the capacitor C2 is discharged. The durative time lies on the quantity of original charge at capacitor C2 before the first charge-sharing occurs. So we need the additional switch M2 controlled by signal **VM** as a guarantee for the capacitor C2 in case of the existing charge.

Because the signal  $VM$  always closes the switch M2 for a short time to discharge the capacitor C2 before the charge sharing occurs, even if at the startup of the circuit, the control circuit is convergent to the correct operation more quickly.

Figure 4a and 4b are simulation results for circuits without and with the switch M2 controlled by signal  $VM$  on the same simulation conditions respectively. In figure 4a, the sampling signal delays several periods compared with the one of figure 4b. The delay time will be longer along with higher capacitance values. Thereby the switch M2 controlled by signal  $VM$  is necessary for the control circuit.

### 5. Characteristics of the novel single-input control circuit

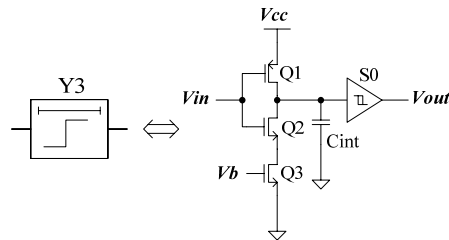
Through the above presentation, the sampling instance can be determined with high accuracy by choosing an appropriate coefficient  $K$ . For example, if we choose the coefficient equals 2, the sampling instance is chosen at about 2/3 of the duration of the voltage pulse at the auxiliary winding. And it is always kept relative constant to the duration of the voltage pulse as long as it is not changed. Thus, high controller accuracy may be achieved. Figure 5 is the relationship between the sampling instance and the duration of the voltage pulse. Y axis is the ratio of sampling instance to the duration. X axis is the duration of the voltage pulse. When the duration is smaller than 20us, the effect of signal  $\Phi a$  is visible. The ratio is bigger than the theoretic value. The accuracy is calculated excepting that range. The standard-deviation is 0.0036 and the accuracy is controlled under an approximate level 1.3%.



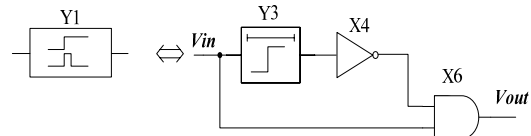
**Figure 5.** Relationship between sampling instance and duration of the voltage pulse

Another characteristic of the novel design is that the width of the sampling signal is adjustable by altering

the value of the internal capacitor. This makes the control circuit available to different sample and hold unit requiring different sampling time. Certainly longer sampling time will result in lower controlling accuracy. So the final result should be a compromise between high accuracy and enough sampling time. Figure 6a and 6b is the circuit diagram of the above-mentioned rising edge delay unit and rising edge pulse generator respectively. The delay time of the rising edge delay unit is determined by its internal capacitor  $C_{int}$  and the bias voltage  $V_b$ . The width of the pulse generated by Y1 is determined by the delay time of rising edge delay unit Y3. So the width of the sampling signal can be adjusted by changing the value of capacitor  $C_{int}$  or the bias voltage  $V_b$ . If the threshold of schmitt trigger S0 is fixed, the width will be longer along with the higher capacitance value or the higher bias voltage.

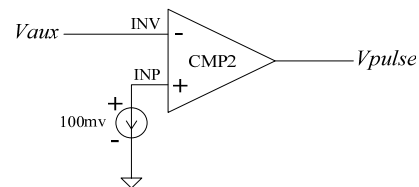


**Figure 6a.** The circuit diagram of rising edge delay unit



**Figure 6b.** The circuit diagram of rising edge pulse generator

The third characteristic of the novel design is that it just needs one input signal whose falling edge represents the beginning of the voltage pulse and rising edge represents the end of the voltage pulse. It is realized easily that only a comparator with a threshold 100mV can satisfy [9]. Figure 7 illustrates such a realization. The input signal  $V_{aux}$  comes from the auxiliary winding in figure 1 and the signal  $V_{pulse}$  outputs to the digital controller of the control circuit in figure 2a.



**Figure 7.** The detection device of the voltage pulse

## 6. Conclusion

Primary-side controlled SMPS are widely used in many applications. As the central part, the design of primary-side controllers is important and challenging. This paper proposes a novel single-input sampling instance control circuit contained in primary-side controllers. According to the design, three characteristics are emerged and satisfy different requirements. The high accuracy guarantees the performance of controllers. The adjustable width of the sampling signal enhances the flexibility of the novel control circuit. And the easy obtaining of the input signal reduces the complication of primary-side controllers. Therefore the novel control circuit is advanced and valuable.

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