Digital Circuits Design Using EDA Experimental System

1Fangqin Ying, 2Xiaoqing Feng
*1College of DongFang, Zhejiang University of Finance & Economics, Zhejiang, Haining, China, 314408, yfq502@126.com
2College of Information, Zhejiang University of Finance & Economics, Hangzhou, China, 310018

Abstract
Electronic Design Automation (EDA) technology represents the development direction of modern electronic design technology. This paper presents the traditional digital circuit design method, carefully introduces a top-down hierarchy design method, analyzes advantages and disadvantages of traditional experimental teaching, and proposes the application of EDA experimentation in digital circuit design. It is comprised of hardware and software. Numerical Control Frequency divider is taken as a typical example to display EDA experimental applications. An EDA experimental system based on FPGA/CPLD can achieve automated design of digital circuit quickly and easily, and thus it provides a good platform for the logic design and development of medium and large-scale digital circuit.

Keywords: Digital Circuit, FPGA, EDA

1. Introduction

The traditional digital circuit uses description tools such as a truth table, Karnaugh map, state equation and state transition table or state transition diagram to design [1]. For a sophisticated digital system which is comprised of tens of or thousands of logic gates, it is difficult, nay, impossible to carry out if using the traditional digital circuit design method. Therefore a much more efficient way of describing and designing digital systems is expected.

Electronic Design Automation (EDA) technology represents the development direction of modern electronic design technology [2]. “top-down” hierarchy design methodology is used usually. This design approach firstly starts from the system design, and the system is divided into several models at the top level. Secondly, each module is implemented by HDL (hardware description language) or schematic entry, and then a comprehensive optimization tool is used, a technology-mapped specific gate circuit netlist is generated [3]. Its corresponding physical implementation can be the programmable logic device. Debugging, simulations are accomplished at high level. It is beneficial to discover an error of structural design in an early phase and avoid the waste of design work. Thus, it not only decreases the workload on logical functional simulation but also enhances accuracy in designing and cuts down the period of the designing. The full design and each module is synthesized in logic, then is simulated in function and timing by EDA software, so hardware/software co-design has been brought to digital logic circuit design.

To keep up with the rapid development of electronic technology, many universities have initiated new courses or updated their existing curricula for microelectronic system design education [4-10]. Our school also intends to develop digital circuit based on EDA experimental systems.

This paper is organized as follows: section 2 introduces the digital logic course; section 3 describes the advantages and disadvantages of traditional digital logic experiments. The experimental system is composed of hardware system and software system which is presented in section 4. The EDA experimental project setting is presented in section 5. The Numerical Control Frequency divider is taken as an example to present EDA experimental applications in section 6, and conclusions and areas of future work are given in section 7.
2. The introduction of the digital logic design

Digital logic is the main course of the computer science and technology major. The main task of the courses is to learn logic algebra, digital circuit, and on the basis of understanding logic gate and common logic devices work principle, and medium scale integrated circuit can be used to design system [11]. The digital logic experiment is an important part of digital logic. Its experimental teaching plays the introductory and leading role in the whole practice teaching system, and also plays an important guiding function for the subsequent practice teaching. Therefore, during the design of experimental teaching it is particularly important to think how to effectively guide students to build engineering thinking method, to grasp the engineering practice skills and to cultivate good practice ability and innovation ability. However, at present, there are quite a few problems in the experimental course of the digital circuit.

3. The advantages and disadvantages of traditional digital logic experiments

Traditional digital logic experiments use breadboard and small or medium-scale integrated circuits to construct circuits, as shown in Figure1. This approach can help students more easily understand and grasp the knowledge of various circuit units, but it is difficult for students to establish links between them and flexibly integrate theory with various practical applications. For instance, the contents of the experimental settings are too old and one fold, the experimental teaching modes are unreasonable, and the implementation process is inflexible and cannot link up with subsequent courses. After completion of the course, students do not understand what the course is, although their teachers have emphasized the significance and the uses of the course in classroom, they can not still master the real meaning of the curriculum from the scattered experimental project, because they have not enough perceptual knowledge and experiences. To be specific, it has the following disadvantages:

A. Low reliability: there are too many connecting wires or connector based on the traditional manual design methods (as shown in Fig.1). As the traditional digital circuits consist of universal logic devices such as 74 series or CMOS 4000 series, the quantity of such devices will greatly increase when the system is designed on a slightly larger scale. Obviously, the fault rate of this system is very high. A mistake in an experimenter’s circuit could cause a serious accident, such as an electric shock or fire [12].

B. Low efficiency, high cost. Since the traditional design of digital circuit is almost based on manual, in which each step of the system design including representation of the design object, logical analysis, logical simplification, schematic drawing, circuit design, as well as the system implementation and test are accomplished by hand. Once the final design does not meet the actual need, the design has to be done all over again from the bottom up. Therefore, even hundreds of logic gates or small scale circuit development cycles are very long. Obviously, promoting efficiency of the design will inevitably lead to cut down design costs and raise product competitiveness.

C. TTL (Transistor-Transistor-Logic) or CMOS (Complementary metal-Oxide-Semiconductor) 74 series logic devices are used to perform the experiment. There are still some weak points of them, such as low-speed, small-scale and high operating voltage, there is very few technical skill associated with modern digital technology. Learners have no way of acquiring some knowledge about the real engineering design.
D. The content of all experiments, experimental methods still remains at the same level as 30 years ago which belong to the small-scale logic system manual design technical areas. Almost all of the technologies involve computer applications. However, analysis, design and verification in the present digital logic textbook do not use the technologies of computer. This lead to means and methods of experiments or the experimental results are very backward.

These traditional systems cannot cope with the broad variety of circuits designed by individual experimenters because they are technologically based on all-purpose or ready-made learning tools. This lead to the learners’ understanding of the design results and design techniques is superficial, surface. Using computer advanced timing simulation tools and logic analyzer can make learners become very transparent to the experimental circuit. It is essentially different from Multisim (electronics workbench). Multisim software dummies a workbench of digital circuit simulating. It supplies user variable elements of digital circuit such as logic gate circuit, coder, encoder, adder, trigger, LED etc. Using these elements, we can build up all digital circuits which have been completed in our laboratory. The elements and instruments we used are close to virtual ones [13]. EWB in actuality is only the functional emulation; it bears no relation to the actual circuit. Therefore practical experience can not be obtained. For all of these reasons, it imminently asks for developing other educational support systems for experiments involving digital circuit construction in order to improve the design level.

4. EDA experimental system

In order to avoid these disadvantages above and make students learn better and faster and deepen the understanding of experimental principle, EDA experimental teaching is presented.

EDA takes the computer as the working platform, the EDA software is its development environment, using hardware description language as design language, while taking the programmable device as the target device, so automated design of electronic systems can be realized. Therefore not only the design scale and function is increased, but also the fundamental transformation in electronic circuit design ideas and methods is accomplished. Thus changes the traditional “on board” design technology from “based on a chip” design. Hardware/software co-design is put forward to digital logic circuit design. Generally speaking, EDA experimental system is composed of hardware system and software system, as shown in Figure 2. (a) and (b).

4.1. Introduction of software system

Altera Corporation’s QuartusII software is mainly used to design its FPGA and CPLD devices. It provides logic design, synthesis, routing, simulation and programming. In a single, standard design environment, it provides a set of tools for synthesis, optimization and validation [14]. Its function is very powerful. It is the most comprehensive design environment which is suitable for development of a single-chip programmable system. A solution for FPGA and CPLD designs can realize in all stages of it. Altera Quartus II design software provides a complete design environment with a multi-platform. It is easy to meet the needs of a specific design.

4.2. Introduction of hardware system

The EDA experiment hardware system is a self-developed board equipped with FPGA chip and various additional hardware components. As shown in Figure 2. In order to flexibly use these resources to design the system, the mother board is designed with commonly used input and output devices such as switches, a keyboard, LEDs and LCDs. All the pins of the devices are connected around the breadboard for easy and customized connection.
4.2.1 Introduction of FPGA chip

Field Programmable Gate Arrays (FPGA) contains a vast number of basic digital components. The interconnections between these components can be defined by a user. FPGAs are reprogrammable devices, where making the change from one digital circuit to another is made by simply downloading a new interconnection file, greatly facilitating the design and debugging of complex digital circuits. FPGAs can be reprogrammed repeatedly. Therefore the user could modify and download the modified design on the same device as many times as he/she wishes. The number of basic components in single FPGA chip has grown significantly making it possible to realize very complex digital circuits on FPGAs [15]. FPGA chip EPIC6Q240C8 product is selected. It is the core hardware of system with 240 pins. Among all the pins, 185 pins can be used as an I/O pin at most. It has two PLL (Phase Locked Loop) of 8ns and 6030 LE, each LE includes a LUT, a trigger and related relevant logic. Look-up table (LUT) is a RAM unit in fact.

4.2.2 Introduction of Peripheral Circuit

1. Key1-Key8: For experimental signal control key, these eight keys are controlled by the “multi-tasking reconfigurable circuit”. Its function in every circuit diagram and its connection with the main system depends on the mode button selection, which can be referred to the block diagram of the experimental circuit for detailed information [16].

2. Digital luminescence tubes1-8/light emitting diode D1~D16: they are controlled by the “multi-tasking reconfigurable circuit, the form of their connections also should be referred to the experimental circuit configuration diagram.

3. The clock frequency selection: Located on the right side of the master system, target chip will obtain different clock frequency signal by changing short circuit cap’s connections. CLOCK0 frequency range: 0.5Hz-50MHz. As clock0 has more optional frequency, it is more suitable for the target chip to choose it as a signal input terminal in the projects of signal frequency or period measurement design. Each frequency source and the corresponding clock input can only be inserted one short circuit, that is to say, this system can only provide four clock frequencies for FPGA: CLOCK0, CLOCK2, CLOCK5, CLOCK9.

4. Speaker: connected with the target chip’s port of speaker, it can make a sound through this port. The Specific corresponding pin number to the target device pin number should be turned to operation manual for further details.

5. PS/2 interface: Through this interface, the PC keyboard or mouse can be connected to the target chip of GW48, so the experiments concerning PS/2 communication and control can be accomplished.

6. VGA video interface: the target chip can control VGA monitor by means of this interface.

7. Single-chip Microcontroller interface: Connection mode with the target board is marked on the main system board.

8. RS-232 serial communication interface: This interface circuit is used for debugging FPGA and PC communications and SOPC or implementing the bidirectional communication with PC, microcontroller, and FPGA / CPLD.

9. D/A Converter: Using this circuit module, the experiments or development of FPGA / CPLD target chip and D / A converter interface can be completed.
5. EDA experimental project setting

In order to raise teaching efficiency and improve teaching quality, it is of prior importance to reform teaching substance, to reduce verifying experiments and to increase comprehensive and designing experiments. The EDA experiments are designed in three different levels according to the learning process or level of different students, as shown in Table 1. The three levels of experiments include simple experiments, general design experiments, and comprehensive experiments. A gradual project-based approach was used to train students’ system design capability step by step. In performing the experiments, students learn the latest EDA technology, hardware/software co-design methodology, and mixed-signal system design methodology.

A. Simple Experiments

These are simple experiments for students to learn and become familiar with EDA features, its development environment, Quartus II tools and understand reconfiguration, EDA concepts and Grasp the application of hardware description language, schematic input method in the design of the circuit. Students choose one or two of the following experiments and finish them independently. Combination logic: Adder, Substractor, Comparator, Decoder, Encoder, Multiplexer. Sequential logic: Latch, Flip-Flop, Counter, Register, Synchronous Circuit, Asynchronous Circuit, Memory Circuit.

<table>
<thead>
<tr>
<th>Level of experiment</th>
<th>Teaching objective</th>
<th>Teaching method</th>
<th>Capability obtained</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simple experiments</td>
<td>Learning EDA features and its development tools</td>
<td>Complete by independently following the instructions</td>
<td>A knowledge of how to perform reconfigurable hardware/software co-design with EDA</td>
</tr>
<tr>
<td>General design experiments</td>
<td>Train students’ system design capability and improve their hardware/software co-design capability</td>
<td>Design and finish independently</td>
<td>A knowledge of how to design a mixed-signal system</td>
</tr>
<tr>
<td>Comprehensive design experiments</td>
<td>Design projects to improve students’ mixed-signal system design capability</td>
<td>Design and finish in team</td>
<td>An ability to design a real mixed-signal project</td>
</tr>
</tbody>
</table>

B. General design experiments

The main purpose of the experiment is to train student’s system design capability and improves their hardware/software co-design capability to give them the knowledge of how to design a mixed-signal system. Through the completion of the general design experiments students can grasp the simple digital logic circuit and system design methodologies and EDA design flow, to learn the use of commonly used peripheral hardware. Students choose one of the given experiments and finish it independently.

C. Comprehensive Experiments

These are real electronic system design projects to improve students’ system design capability. Students choose one of the following four projects and finish it as part of a team. This includes music performance circuit, digital frequency meter, VGA controller, and competition responder. This electric circuit experimental realization and the control logic are complex, so it requires the ability to design a real mixed-signal project.

6. Typical experiment

“Numerical Control Frequency divider” is taken as an example to illustrate our exploration in integrating the modern EDA technology into digital circuit’s experiment.

The experimental process is divided into three stages: system design, programming and download commissioning. In the system design stage, using top-down design methodology for system design. Firstly, the designer should analyze requirements of the system, determine complete function and main performance index of the system, draw the block diagram of the system, and indicate the input and output signal. Secondly, determine the principle and methods of the system logic functions, divide system into several models. During each phase of the design process, a variety of input methods such as: HDL (Including VHDL, VerilogHDL, ABEL, AHDL and other hardware description languages), schematic entry can be used. Quartus II is used as a software to edit HDL file, compile, and utilize its
simulation tools Simulator to carry out functional or timing simulations to ensure logical validity. Execute function simulation, connecting the various subsystems which passing compilation and simulation so as to compilation and simulation of the overall system, download and hardware test after guaranteeing the simulation waveform is done correctly. After connecting the power supply, notice whether the test result fills the demand of design. If not, to modify the subsystem or the top circuit design according to the test case, recompiling and re-simulating until the test result receives good effects in experiment.

6.1. EDA experimental applications- Numerical Control Frequency divider

The function of Numerical Control Frequency (NCF) divider is to generate a different dividing coefficient frequency signal with different input data entries and make the frequency of the output signal to be a certain function of input data [17]. It is widely used in digital electronic systems. The traditional method to design NCF divider is using the universal counter chip with the preset data input, its design procedure and circuit are quite complex. Especially when the frequency dividing coefficients is large, it needs multiple integrated counter chips and more complicated control circuits to achieve. Moreover, it has poor flexibility and portability.

Now, NCF divider is developed based on VHDL, which is a kind of IEEE industrial standard modeling language, because VHDL has strong capability of behavioral description, systems description and hierarchical program structures. If NCF divider is used as a module, it can also be ported in a lot of digital circuit systems and modify easily. Just altering a few sentences in the program, the maximum frequency coefficient can be changed; the whole design process is simple and effective. Moreover, hardware and platform independence of VHDL make it is easy to download to all kinds of programmable logical device.

6.2. Design principle of NCF divider

Figure 3. RTL (Register-Transfer-Level) Circuit Diagram

Up counter is counted based on parallel presetting. It produces preset data inputting control signal when the count value overflows, load preset data at the rising edge of the clock signal and overflow signal is used as the divider output signal. Therefore, a different frequency signal output is achieved. Under the development flat of Quartus II, top- down and hierarchy design circuit diagram are adopted as shown in Figure 3. Algorithm involved in software design is carried out in VHDL as shown in Figure 4.
After successfully compiled as shown in Figure 5, the next step software simulation and hardware verification can be executed. If there are any errors, algorithm should be revised until it having been successfully compiled.

6.3. Software Simulation and Hardware Verification

Quartus II has the great advantage of powerful simulation and analysis capabilities. Therefore, at each stage of the design process, we can utilize Quartus II simulation tools to carry out functional or timing simulations on our designing circuits to ensure logical correctness. This is one of the significant advantages of EDA technology. Figure 6 shows the simulation waveform of NCF divider. It can be seen from figure that when input D is different, the frequency of output FOUT changes.

After the software simulations of all the modules in Quartus II have been finished, we can perform hardware verification on the designed circuit. The first step of hardware verification is to assign pin for each I/O port of the top-level circuit shown in Figure 7.
Then, some settings should be made, such as: select mode1; keys 1, 2 are responsible for inputting the eight preset number D; CLK is inputted by CLOCK0, which Frequency is 65536Hz. Output FOUT is connected with the Speaker. Finally, download .sof file into the EDA experimental development system through the download cable. Change the input value of the key 1 or key2, different voices can be heard. The experiment results show that the performance of the system is excellent.

7. Conclusion and future work

This paper firstly presents a top-down and hierarchy method of modern electronic technology. Then, the disadvantages of traditional digital circuit experiment system are analyzed and QUARTUS II EDA tool of ALTERA Corp and FPGA based digital circuit experiment system is presented. It focuses on the experimental design method and presents a three-stage experiment according to the learning process or level of different students. The proposed experiment system can achieve most of the functions that traditional experiment instruments can do and cannot do and improve the learning effectiveness. Based on the EDA experimental system, we plan to make further researches into remote labs and remote-teaching into our digital circuit experiment courses. The remote laboratory system is to realize an internet based remote digital logic circuit experiment, which enables efficient sharing of test equipments both in space and time division fashions as well as supporting many users to perform experiments concurrently.

References


