A 1.2 V, CMOS Differential Low Noise Amplifier with Low Noise Low Power for Bluetooth Receiver

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Abstract

A differential Low-noise Amplifier (DLNA) using 0.13 µm CMOS technology is presented. The amplifier is optimized for Bluetooth Receiver applications operating in the 2.4 - 2.5 GHz band. The inductive degeneration topology used in the DLNA provides low noise, high gain and a large IIP3. The differential LNA was added a cascade output stage to the Single-ended source degenerated stage. Simulation was made by using the Advanced Design System (ADS) software. The proposed differential LNA is consuming 31.66 mA current at 1.2V supply voltage, it exhibits a linear gain of more than 24.725 dB, noise figure of 1.91 dB, input return loss (S11) of -5 dB, S12 of -80 dB and an IIP3 of -11 dBm.

Keywords: Differential LNA; Noise Figure; stability; IIP3; Bluetooth applications; Low power; S parameters.

1. Introduction

During the last decade, the increasing demand of wireless communication systems with lower cost, small size, low power and high performance than ever, and this drives IC designers to innovate new circuit topologies. A wireless communication papers on amplifiers network consists of a set of devices or nodes that carry out basic networking functions [13]. The goal in building RF receiver IC’s is that has high sensitivity, wide dynamic range, low power consumption and to reduce the number of off-chip passive components in the circuit. Many studies and published are released on amplifier [14-15]. Low noise amplifier (LNA) which is in the RF front-end circuit has the great value in this field [1-3]. LNAs are a crucial component of RF receivers. The principle effect of LNA is to amplify the weak signal which is received by the antenna. It should provide enough gain, Low noise figure (NF), great input and output matching, a high linearity and Stability factor (K factor). Differential structures have the following advantages compared to single-ended topologies, such as insensitive to the noise and interference coupled through supply lines and substrate. Many linearization methods used for transconductance stages can also be used for low noise amplifiers and filters using this approach, and differential signal can be used to eliminate the negative effect of leaking signal.

In this paper, we present a design of 2.4-2.5GHz-band CMOS DLNA optimized for Bluetooth application. Our purpose is to improve the performance of DLNA. The emphasis of this study is to reduce the power consumption of the CMOS LNA while still retaining acceptable noise performance, good input/ output match, sufficient linearity, and a high dynamic range. A cascode amplifier topology with inductive degeneration at the source was used. The LNA offered NFs of 1.91 dB and input return losses of -5dB, reverse isolation of -80 dB, input ICP1 of -30 dBm and IIP3 of -11 dBm with power consumptions of 38 mW.

Figure 1. Block diagram of a Bluetooth receiver
2. DLNA Circuit Design

2.1. Differential LNA Topology

Figure 2. Schematic of a Single-ended source inductive degeneration LNA

Figure 2 shows a schematic of a single source–inductor–feedback amplifier with the gate inductor for input impedance matching. The source inductor is used to achieve simultaneous input and noise matching [4]–[5] and to provide the desired input resistance 50Ω [6]. The cascode structure is a combination of a common–gate load. This has the effect of increasing the output impedance. The additional cascode device has been configured as a diode. The inductor between the cascode source and supply blocks any RF is leaking to the supply rail and maybe varied in value to optimize the gain response of the LNA. Figure 2 represents a half of final differential DLNA. The topology is matched to a 50 Ω source using the inductive Degeneration Ls. This is often expressed by the parameter S11. The expression of input impedance is defined in (1)

\[ Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gs} + g_m/C_{gs}} \approx s(L_s + L_g) + \frac{1}{sC_{gs} + W_L} \]  \hspace{1cm} (1)

To achieve input matching, the \( Z_{in} \) should be 50 Ω, so

\[ Z_{in} = \frac{g_m}{C_{gs} L_s} \]  \hspace{1cm} (2)

The value of \( L_s \) is picked and the values of \( g_m \) and \( C_{gs} \) are calculated to give the required \( Z_{in} \).

2.2. Differential LNA Circuit Design

The design circuit of the differential LNA is shown in Figure 3. There is many advantages of DLNA over single-ended LNA. Firstly, DLNA offers a stable reference point. Secondly, the differential LNA reduces the noise. Thirdly, the use of Gilbert mixers and image rejection schemes require to be fed from a differential source. The differential amplification of the signal ensures an attenuation of the common mode signal, in most systems this common mode signal will be noise.
The virtual ground formed at the tail removes the sensitivity to parasitic ground inductances which makes the real part of the input impedance purely controlled by \( L_s \) [7]. The differential input voltage is supplied via the balun transformer (CMP1). An ideal current source has been added at this stage on the ‘tail’.

### 3. Simulation results

ADS simulations for the DLNA were done using 0.13 um CMOS process. The differential amplifier provides a maximum gain of 24.725 dB at 2.4 GHz as shown in figure 4. This circuit operated with 1.2 V supply. The reverse isolation S12 (Fig.5) is good with more than – 80 dB. Minimum noise figures of 1.91 dB and 1.97 dB are obtained around the desired frequency 2.4-2.5 GHz for the designed DLNA’s as shown in figure 7.

![Figure 4. ADS Simulation characteristics of gain (S21)](image_url)
According to the meaning of the stability figure

\[
K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{221}S_{12}|}
\]

\[
\Delta = |S_{11}S_{22} - S_{12}S_{21}|
\]

Where \(K>1\), that \(\Delta<1\) the circuit is stable unconditionally.
In order to determine the parameters of linearity we consider the DLNA as a Black box. We obtain an input ICP1 of -30 dBm and IIP3 of -11 dBm as shown in figure 8.

These results demonstrate that high dynamic range and good linearity have also been achieved. A summary of the simulated amplifier characteristics is also included in Table 1.

From Table I, it is clear that the performance of our CMOS LNA are the best reported values among the 2.4-2.5 GHz band CMOS DLNA's compared to some other characteristic.
Table 1. Classical values for CMOS DLNA

<table>
<thead>
<tr>
<th>[Ref]</th>
<th>NF (dB)</th>
<th>Gain (dB)</th>
<th>IIP3 (dBm)</th>
<th>Power (mW)</th>
<th>F0 (GHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[8]</td>
<td>4.7-5.7</td>
<td>16</td>
<td>-</td>
<td>38</td>
<td>2.5-5.2</td>
</tr>
<tr>
<td>[9]</td>
<td>2.6</td>
<td>30</td>
<td>-</td>
<td>3.6</td>
<td>2.4</td>
</tr>
<tr>
<td>[10]</td>
<td>3.5</td>
<td>15.6</td>
<td>-</td>
<td>21</td>
<td>0.2-5.2</td>
</tr>
<tr>
<td>[11]</td>
<td>2.4</td>
<td>18.67</td>
<td>-2.8</td>
<td>16.2</td>
<td>2.0</td>
</tr>
<tr>
<td>[12]</td>
<td>3.4</td>
<td>13-17.5</td>
<td>9.98</td>
<td>0.8-1.7</td>
<td></td>
</tr>
<tr>
<td>This work</td>
<td>1.91</td>
<td>24.3725</td>
<td>-11</td>
<td>38</td>
<td>2.4-2.5</td>
</tr>
</tbody>
</table>

4. Conclusion

In this paper we proposed a 2.4-2.5 GHz CMOS DLNA. Simulation results show that from a supply of 1.2 V, the DLNA achieves a power gain (S21) of 24.725 and maximum Noise Figure (NF) of 1.97 dB. A power consumption of 38 mW has been attained to meet the required specifications of CMOS DLNA. Good noise and gain performances were obtained. Also, a high IIP3 of -30 dBm, which shows the good linearity characteristics, was proved by several simulations.

5. References


