A 0.18μm CMOS Based Programmable Integer-Fractional Combined Frequency Divider for Frequency Synthesizer of Multi-Standard Wireless Systems

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Abstract

This paper first presents the architecture of a frequency synthesizer which can support multi-standard wireless systems of GPS, Galileo, and WCDMA standards. Then, a programmable integer/fractional combined frequency divider (CFD), which is the key building block of the proposed frequency synthesizer, is designed and implemented by using 0.18μm RF CMOS process. The CFD mainly consists of an integer-N frequency divider and a 3rd ΔΣ modulator for fractional frequency division. The integer-N frequency divider is based on pulse-swallow counter-type architecture to allow division ratio range from 512 to 767. For 3rd ΔΣ modulator, the state of art Multi-Stage-Noise-Shaping (MASH) 1-1-1 structure is used for good shaping of quantization noise. With a 1.8V voltage supply, the CFD exhibits an operating frequency range from 0.5 to 6GHz and draws a current of 2.2mA at the input frequency of 4.5GHz. The measurement results indicate that the programmable integer/fractional combined frequency divider works well and can be used for the proposed multi-standard frequency synthesizer.

Keywords: Frequency Divider, MASH 1-1-1, Pulse-Swallow Counter, Multi-standard frequency synthesizer

1. Introduction

Currently, the market of satellite navigation is dominated by the global positioning system (GPS), but other satellite navigation systems will soon be available such as Galileo system being developed by the European Union. Moreover, the Federal Communications Commission (FCC) regulation (Enhanced 911) has also state that every cellular devices should be capable of determining the location with better than 100-meters accuracy [1-3]. Take all this into account, for accurate positioning including inside building or personal navigation environments, hybrid GPS/Galileo receivers in combination with cellular network positioning capability, which provide seamless indoor/outdoor navigation and communication capability, are attracting more and more attentions.

One big challenge to realization of such hybrid receiver is the design of a multi-standard frequency synthesizer that is able to generate clean and stable local oscillator (LO) signals fulfilling the stringent performance requirements. In addition, key points for a multi-standard solution are the minimization of the silicon area and of the power consumption, which lead to maximum hardware sharing. Although the problem can be addressed at different hierarchies in the design flow, it is best tackled by selecting a frequency synthesizer architecture that is well suitable for a multi-standard implementation.

A straightforward approach is to parallelize multiple separate frequency synthesizers [4], but it wastes significant chip area and power consumption. Another approach is to use additional frequency processing such as frequency division, frequency multiplication, and mixing functions to generate the desired frequency [5]. This technique requires additional processing circuitries which is not effective for power and area saving and also suffers from poor spectral purity and high phase noise.

To reduce the cost, area, and power consumption, a programmable integer/fractional combined frequency synthesizer (CFD) architecture capable of implementing multiple standards on a single phase-locked-loop (PLL) with maximum component sharing is presented. The frequency synthesizer is able to reconfigure between integer mode for GPS/Galileo and fractional mode for WCDMA. The key aspects in achieving the specs in a fully integrated fashion are a programmable integer/fractional CFD together with variable reference frequency, as will be discussed in the subsequent sections.
This paper is organized as follows. Firstly, the architecture of the proposed GPS/Galileo/WCDMA frequency synthesizer with maximum hardware sharing is presented. And then, a programmable integer/fractional combined frequency divider, which supports integer and fractional frequency division, is designed and implemented by using 0.18μm RF CMOS process. Measurement results indicate that it works well and can be employed in the proposed GPS/Galileo/WCDMA frequency synthesizer.

2. Proposed frequency synthesizer architecture

In our design, the frequency synthesizer is designed for a hybrid Zero-IF and Low-IF receiver, in which a zero-IF architecture is configured for WCDMA and low-IF architecture for GPS/Galileo with IF frequency of 20.46MHz. Some specifications of the frequency synthesizer designed for GPS/Galileo/WCDMA are listed in Table 1. These standards are very different in the frequency range and frequency resolution.

![Table 1. Specifications for the frequency synthesizer](image)

<table>
<thead>
<tr>
<th>Standard</th>
<th>Frequency (MHz)</th>
<th>Resolution</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPS/Galileo</td>
<td>L1/E1 1554.98</td>
<td>1.023MHz</td>
</tr>
<tr>
<td></td>
<td>L5/E5a 1555.99</td>
<td></td>
</tr>
<tr>
<td></td>
<td>E5b 1186.68</td>
<td></td>
</tr>
<tr>
<td>WCDMA</td>
<td>2100–2170</td>
<td>200kHz</td>
</tr>
</tbody>
</table>

To meet the frequency resolution of all standards simultaneously, two integer-N PLLs with 1.023MHz and 200 kHz reference frequency would require division ratio N in excess of 1000 and 10000, respectively. Such a high N leads to a high in-band phase noise and charge-pump (CP) current. Compared to integer-N architecture, the fractional one allows a potentially arbitrary output frequency resolution and more freedom in the reference frequency choice while a single PLL is adopted. However, it suffers from a major drawback called fractional spur. On the other hand, since multi-standard usually means wide output frequency range, it would be result in very different frequency division ratio if a single reference frequency was used. As shown in the following equation, the closed-loop bandwidth of the PLL, \( \omega_{3\text{dB}} \), can be approximated by [6]

\[
\omega_{3\text{dB}} \approx \frac{I_{CP} \cdot K_{VCO} \cdot R_2}{2\pi N R_2}
\]  

Where \( R_2 \) is the loop filter resistor, \( K_{VCO} \) is tuning-gain of voltage-controlled-oscillator (VCO), and \( I_{CP} \) is the CP current. Note that \( \omega_{3\text{dB}} \) is proportional to the reciprocal ratio of N. Large variation of N results in a PLL loop bandwidth that varies significantly with it. It gives problems for the loop stability and brings difficult to optimization of phase noise performance as well as lock time. So, in order to compensate the variation of loop bandwidth, either charge pump or loop filter would need to be designed individually. That complicates the design and isn’t effective for power and area saving.

Figure 1 illustrates the architecture of the proposed multi-standard synthesizer, which is based on a single PLL. In order to avoid VCO pulling, a multi-band VCO is used as an oscillation source, and it is combined with divide-by-2 divider to synthesize the wide frequency range for GPS/Galileo/WCDMA. To maximize hardware sharing, a programmable integer/fractional combined frequency divider is employed.

Correspondingly, the frequency synthesizer has two modes, i.e. integer mode and fractional mode. For GPS/Galileo, an integer divider is used, with the reference frequency of 4.092MHz, leading to frequency division ratio of 760, 565, and 580 for GPS L1/Galileo E1, GPS L5/Galileo E5a, and Galileo E5b, respectively. For WCDMA, the integer divider is in combination with a 3rd \( \Delta-Sigma \) modulator with 20-bit input so that the fractional division ratio can be obtained with the reference frequency of 8.184MHz, approximately with 8kHz frequency resolution, and the requiring integer division ratio range from 513 to 533.
To use a single external crystal oscillator of 16.638MHz, which is typically used in stand-alone GPS application, two frequency dividers with divider ratios of 4 and 2 are used for integer mode and fractional mode, respectively. Channel selection and other control signal are provided through serial interface.

Since the reference frequency and division ratio are chosen closely for two modes, similar loop bandwidth of the PLL can be obtained, and the charge pump and loop filter become shared components, and the integration of frequency synthesizer is improved and the chip size is saved.

3. Design and implementation of the programmable integer-fractional combined frequency divider (CFP)

Figure 2 shows the block diagram of the proposed programmable integer/fractional combined frequency divider (CFD). As the key building block in the proposed frequency synthesizer, it consists of an integer-N frequency divider, a 3rd ΔΣ modulator, and control circuit necessary for mode and channel selection. The operational mode is selected according to mode select signal (MS) value: integer mode (MS=1) or fractional mode (MS=0).

3.1. Integer-N frequency divider

For integer-N frequency divider, pulse swallow architecture is adopted since it allows wideband operation together with high operating frequency and low power consumption. As shown in Figure 2, a dual-modulus prescaler (DMP) is in combination with two programmable counters (pulse counter and swallow counter) to realize an integer-N frequency divider. The swallow counter is used to control the DMP which is set to either N or N+1. If the mode control signal (MC) is set to be ‘high’, the prescaler is divided by N, otherwise N+1. The modulus of pulse counter is P and the modulus of swallow counter is S. In order to work properly, P must be larger than S, and both of them can be configured.

Figure 1. Proposed frequency synthesizer architecture

Figure 2. Proposed integer/fractional CFD
According to certain division ratio. At the initial reset state, the DMP is set to a division ratio of \(N+1\), but the swallow counter will change this division ratio to \(N\) while it counts up to \(S\), and then, pulse counter continues to count up while swallow counter stops working. Until pulse counter counts to \(P\), a division cycle is finished and both counters are cleared to zero for next division period. So the division ratio can be expressed as follows:

\[
M = S \times (N+1) + (P-S) \times N = P \times N + S
\]  

(2)

According to (2), in order to cover our required division ratio, different \(P\) and \(S\) can be obtained as shown in Table 2.

<table>
<thead>
<tr>
<th>(M = P \cdot S + N)</th>
<th>(P)</th>
<th>(S)</th>
</tr>
</thead>
<tbody>
<tr>
<td>513</td>
<td>32(100000)</td>
<td>1(0001)</td>
</tr>
<tr>
<td>514</td>
<td>32(100000)</td>
<td>2(0002)</td>
</tr>
<tr>
<td>\ldots</td>
<td>\ldots</td>
<td>\ldots</td>
</tr>
<tr>
<td>527</td>
<td>32(100000)</td>
<td>15(1111)</td>
</tr>
<tr>
<td>528</td>
<td>33(100001)</td>
<td>0(0000)</td>
</tr>
<tr>
<td>\ldots</td>
<td>\ldots</td>
<td>\ldots</td>
</tr>
<tr>
<td>533</td>
<td>33(100001)</td>
<td>5(0101)</td>
</tr>
<tr>
<td>565</td>
<td>35(100011)</td>
<td>5(0101)</td>
</tr>
<tr>
<td>580</td>
<td>36(100100)</td>
<td>4(0100)</td>
</tr>
<tr>
<td>760</td>
<td>47(101111)</td>
<td>8(1000)</td>
</tr>
</tbody>
</table>

3.2. Divide-by-16/17 dual-modulus prescaler (DMP)

The schematic of divide-by-16/17 dual-modulus prescaler is shown in Figure 3. It is built up with two D-flip-flops (DFF), three toggle-flip-flops (TFF), and several gates. Depend on the logic value at control signal \(MC\), the first stage division ratio is two (\(MC=1\)) or three (\(MC=0\)). The operation speed of the DMP is mainly limited by that of the synchronous divide-by-2/3 counter, which is the part operating at the maximum frequency [7]. To maximize the speed of it, the source-coupled-logic (SCL) configuration is adopted for the DFF due to its high-frequency characteristic. Meanwhile, the OR gate and DFF are merged together for shorting delay time [8], and the tail current is removed for less power consumption as well as larger output voltage swing.

As shown in Figure 3, the output of the synchronous counter is directly connected to the asynchronous divide-by-8 counter. The operating frequency of the divider-by-8 counter is two or three lower than that of the divider-by-2/3 counter. Therefore, the optimization of TFF in this stage is focused on the reduction of the power consumption. So the dynamic TSPC DFF [9] is used to diminish the overall power consumption.

![Figure 3. Schematic of the 16/17 dual-modulus prescaler](image-url)
3.3. Pulse counter and swallow counter

Since two counters work at much lower frequency than DMP prescaler which maximum frequency is about 280MHz in our design, standard cell design based on the Artisan 0.18μm standard cell library is used to simplify the design cycle. The use of a standard cell library offers shorter design time, induces fewer errors in the design process, and is easier to maintain.

3.4. 3rd Δ-Σ modulator

To accomplish fractional division, a Δ-Σ modulator is added to modulate the integer-N frequency divider so that the fractional frequency step resolution can be obtained by changing the division modulus factor with the output sequence from the Δ-Σ modulator. The division ratio alterations take place very rapidly in a random/pseudo-random fashion and the instantaneous division is the sum of a base integer N, and the integer output of the Δ-Σ modulator, \( n(t) \), so the average fractional division ratio can be expressed as follows:

\[
N_{\text{frac}} = N + n(t) \tag{3}
\]

Where \( n(t) = K/2^k \) is the average output of the Δ-Σ modulator, and \( k \) is the number of bits of the Δ-Σ modulator while \( K \) represents the input number to the Δ-Σ modulator. In our design, 20 bits is selected for fine frequency resolution as well as superior performance.

An important issue must be considered in the Δ-Σ modulator is the contribution of quantization noise to the synthesizer’s spectral purity. Since the intrinsic division ratio of the integer-N divider is still an integer, the quantization noise is inevitably introduced and behaves in a periodic manner [10]. To resolve the problem, maximize the output sequence length of the Δ-Σ modulator is required.

Although the traditional high-order Multi-Stage-Noise-Shaping (MASH) structure performs higher order noise shaping, it still suffers from spurs in the output spectrum since the output sequence length can be very short for some input values and initial conditions. In this paper, we implement the state of the art MASH 1-1-1 structure, as was proposed and described in [11], that totally stands in matching the input value and the output average and provides long output sequence lengths for the full input range.

As shown in Figure 4(a), the proposed MASH 1-1-1 structure cascades error-feedback-modulator (EFM) which is similar to the traditional one but has an additional feed-forward connection between adjacent stages. It cascades three EFMs by connecting both the output and the quantization error to the input of next-stage EFM. Each EFM constituting the proposed MASH 1-1-1 take two inputs and generates two outputs to be fed to the next EFM, as shown in Figure 4(b).

![Figure 4. (a) Proposed MASH 1-1-1 structure; (b) Proposed EFM structure of each stage](image)

To verify the functionality of the proposed MASH 1-1-1, a structural gate-level model is developed in MATLAB simulink and is simulated for all possible static input value. In addition, a conventional MASH 1-1-1 is also constructed for comparison purpose. With the same input value, the output power spectrum of the proposed MASH 1-1-1 and the conventional MASH 1-1-1 are calculated, as shown in Figure 5, while the dashed line represents the theory NTF curve.
Note that the spectral characteristic of the proposed MASH 1-1-1 is similar to the conventional one. Both of them are shaped smoothly by the Noise-Transfer-Function (NTF). However, it is evident from the figure that the proposed MASH 1-1-1 has better quantization noise performance than the conventional MASH 1-1-1 due to smoother spectrum. This is as excepted as the output sequence length of the former is longer than that of the latter.

![Figure 5. Output spectrum of the proposed MASH 1-1-1](image)

For speed up purpose and hardware complexity, four cascaded 5-bit carry-skip-ahead (CSA) adders are used to realize the 20-bit adder. A 1-bit register is inserted between each CSA stage to pipeline the 20-bit adder. In addition to this, we also add additional 5-bit register to provide time alignment between the input and the output. The bits of both inputs of the adder should be appropriated delayed to synchronize them with the true carry signals, conversely, the output bits are realigned in time by likewise employing the appropriate delays.

4. Measurement results

The circuit has been fabricated with a 0.18μm RF CMOS process and the chip microphotograph is shown in Figure 6. The performance of the fabricated programmable integer/ fractional combined frequency divider is evaluated on wafer by employing a Cascade Microtech probe station. The differential inputs are provided by Rohde & Schwarz SMP04 signal generator. The outputs are monitored on an oscilloscope and an Agilent E4440A spectrum analyzer.

![Figure 6. Die photo of the proposed CFD](image)

Under a supply voltage of 1.8V, the integer/fractional CFD exhibits an operating frequency range from 0.5 to 6GHz. Measured minimum input power at different input frequencies is shown in Figure 7. For integer mode, an integer division ratio of 532 is set.

Figure 8 shows the measured output waveforms of the integer/fractional CFD when an input frequency of 4.5GHz is applied, and the current consumption is 2.2mA. For fractional mode, a
fractional division ratio of \( \frac{532}{2^{30}} \), which means a input value of 551197 to the 3rd Δ-Σ modulator, is set. Figure 9 shows the measured output spectrum when an input frequency of 3GHz is applied. It can be seen that the output frequency is 5.634MHz, corresponding to the right fractional division ratio.

![Figure 7. Measured minimum input power](image1)

![Figure 8. Measured outputs with ratio 532 at input frequency of 4.5GHz](image2)

![Figure 9. Measured output spectrum at input frequency of 3GHz](image3)
5. Conclusion

A programmable integer/fractional combined frequency divider, as the key building block of the proposed multi-standard frequency synthesizer, is designed and implemented by using 0.18μm RF CMOS process. Under a supply voltage of 1.8V, the integer/fractional combined frequency divider exhibits an operating frequency range from 0.5 to 6GHz, and draws a current of 2.2mA when an input frequency of 4.5GHz is applied. Measurement results also show that it works well and can be employed in the proposed frequency synthesizer for multi-standard wireless systems as of GPS/Galileo satellite navigation system and WCDMA cellular mobile communications system.

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7. References